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Regulation of DC Link Voltages of Inverter based STATCOM

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Abstract: In this paper, a static var compensation scheme is proposed for a cascaded two-level inverter-based multilevel inverter. The topology uses standard two-level inverters to achieve multilevel operation. The dc-link voltages of the inverters are regulated at asymmetrical levels to obtain four-level operation. A simple static var compensating scheme using a cascaded two-level inverter-based multilevel inverter is proposed. The topology consists of two standard two-level inverters connected in cascade through open-end windings of a three-phase transformer. The dc-link voltages of the inverters are regulated at different levels to obtain four-level operation. The simulation study is carried out in MATLAB/SIMULINK to predict the performance of the proposed scheme under balanced and unbalanced supply-voltage conditions. A laboratory prototype is developed to validate the simulation results.

Keywords: DC-link voltage balance, multilevel inverter, power quality (PQ), static compensator (STATCOM).

I. INTRODUCTION

In recent years, the custom power technology, the low-voltage counterpart of the more widely known flexible ac transmission system (FACTS) technology, aimed at high-voltage power transmission applications, has emerged as a credible solution to solve many of the problems relating to continuity of supply at the end-user level. Generally, in high-power applications, var compensation is achieved using multilevel inverters . These inverters consist of a large number of dc sources which are usually realized by capacitors. Hence, the converters draw a small amount of active power to maintain dc voltage of capacitors and to compensate the losses in the converter. However, due to mismatch in conduction and switching losses of the switching devices, the capacitors voltages are unbalanced.

Static var compensation by cascading conventional multilevel/two level inverters is an attractive solution for high-power applications. The topology consists of standard multilevel/two level inverters connected in cascade through open-end windings of a three-phase transformer. Such topologies are popular in high-power drives. One of the advantages of this topology is that by maintaining asymmetric voltages at the dc links of the inverters, the number of levels in the output voltage waveform can be increased. From the detailed simulation and experimentation, it is found that the dc-link voltages of two inverters collapse for certain operating conditions when there is a sudden change in reference current. In order to investigate the behavior of the converter, the complete dynamic model of the system is developed from the equivalent circuit. The model is linearized and transfer functions are derived. Using the transfer functions, system behavior is analyzed for different operating conditions.

II. CASCADED TWO-LEVEL INVERTER-BASED MULTILEVEL STATCOM

Fig. 1 shows the power system model considered in this paper. Fig. 2 shows the circuit topology of the cascaded two-level inverter-based multilevel STATCOM using standard two-level inverters. The inverters are connected on the low-voltage (LV) side of the transformer and the high-voltage (HV) side is connected to the grid.

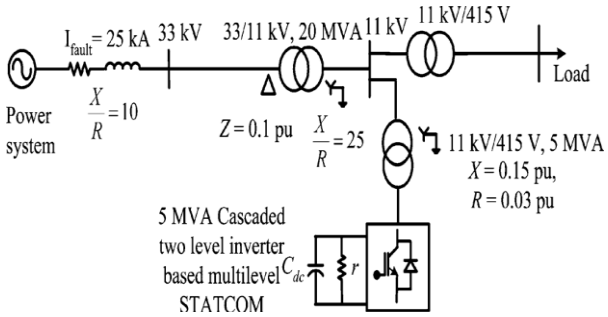

Fig1 Power system and the STATCOM model

The dc-link voltages of the inverters are maintained constant and modulation indices are controlled to achieve the required objective. The proposed control scheme is derived from the ac side of the equivalent circuit which is shown in Fig. 3. Equation (1) represents the mathematical model of the cascaded two-level inverter-based multilevel STATCOM in the stationary reference frame.

$$\begin{bmatrix} \frac{di_a'}{dt} \\ \frac{di_b'}{dt} \\ \frac{di_c'}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-r}{L} & 0 & \\ 0 & \frac{-r}{L} & \frac{-r}{L} \\ 0 & 0 & \end{bmatrix} \begin{bmatrix} i_a' \\ i_b' \\ i_c' \end{bmatrix} \begin{bmatrix} v_a' - (e_{a1} - e_{a2}) \\ v_b' - (e_{b1} - e_{b2}) \\ v_c' - (e_{c1} - e_{c2}) \end{bmatrix}. \quad (1)$$

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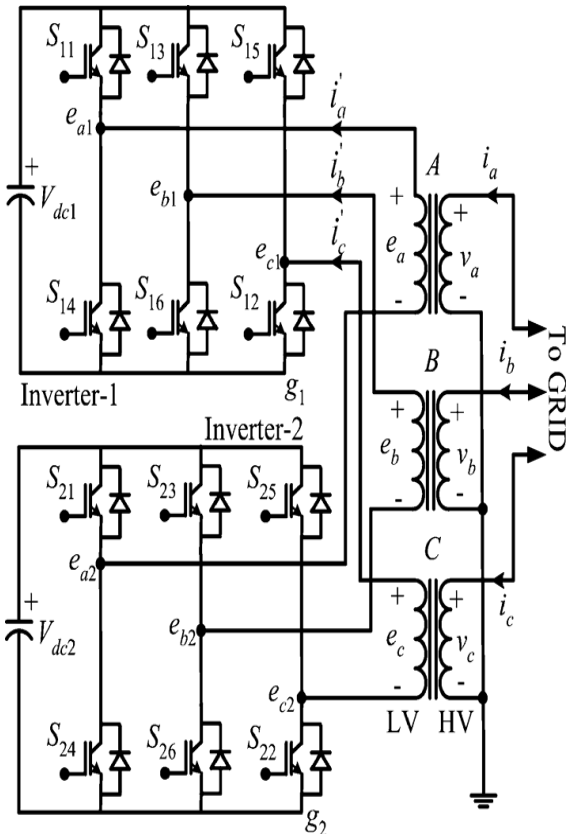

Fig. 2. Cascaded two-level inverter-based multilevel STATCOM

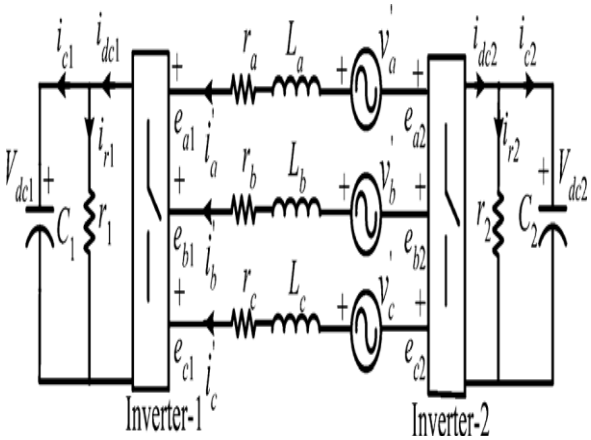

Fig. 3. Equivalent circuit of the cascaded two-level inverter-based multilevel STATCOM.

A. Control Strategy

The control block diagram is shown in Fig. 4. The converter currents are transformed to the synchronous rotating reference frame using the unit signals. The switching frequency ripple in the converter current components is eliminated using a low-pass filter (LPF).

The dc-link voltages of the inverters are maintained constant and modulation indices are controlled to achieve the required objective. The dc-link voltages of two inverters collapse for certain operating conditions when there is a sudden change in reference current. In order to investigate the behaviour of the converter, the complete dynamic model of the system is developed from the equivalent circuit. The model is linearized and transfer functions are derived from proposed system.

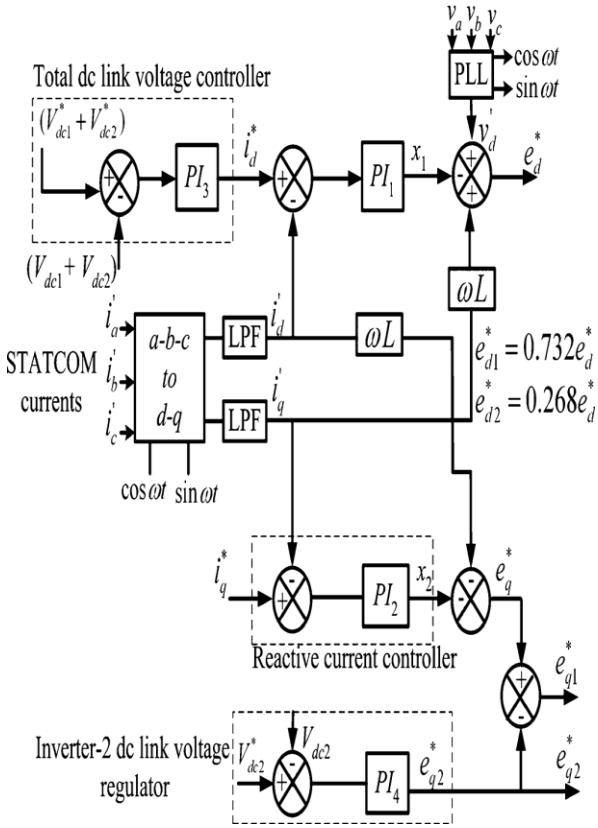

Fig. 4. Control block diagram.

However, this will not ensure that individual dc-link voltages are controlled at their respective reference values. Hence, additional control is required to regulate individual dc-link voltages of the inverters.

B. DC-Link Balance Controller

The resulting voltage of the cascaded converter can be given e1 = $\sqrt{e_d^2 + e_q^2}$ and angle S = $\tan^{-1}((e_q)/(e_d))$

The active power transfer between the source and inverter depends on and is usually small in the inverters supplying var to the grid. Hence, can be assumed to be proportional to .Therefore, the q-axis reference voltage component of inverter-2 is derived to control the dc-link voltage of inverter-2.

The error so obtained is passed through the proportional plus low-pass-filtered derivative controller to produce a switching function. The s-domain representation of the controller transfer function between the output switching function and the input error function. The constants and are the proportional and derivative gains, respectively. The derivative action is associated with the first-order low-pass

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filter to limit the application of the high-frequency noise and disturbances. The low-pass filtering action depends upon the filter coefficients.

The effect of the high-frequency switching due to modulation is modeled as a first-order lag. Therefore, in steady state, the modulation process is defined by a transfer function that consists of a fixed gain and a 1 + TdS delay function.

III. DC-LINK BALANCE CONTROLLER

The active power transfer between the source and inverter depends on and is usually small in the inverters supplying var to the grid. Therefore, the Q -axis reference voltage component of inverter-2is derived to control the dc-link voltage of inverter-2 as, The -axis reference voltage component of inverter-1 is obtained as

$$e1 = ed2 + eq2 \ldots\ldots\ldots \quad (3)$$

It results in four-level operation in the output voltage and improves the harmonic spectrum. The reference voltages generated for inverter-2 are in phase opposition to that of inverter-1. From the reference voltages, gate signals are generated using the sinusoidal pulse-width modulation (PWM) technique. Since the two inverters' reference voltages are in phase opposition, the predominant harmonic appears at double the switching frequency.

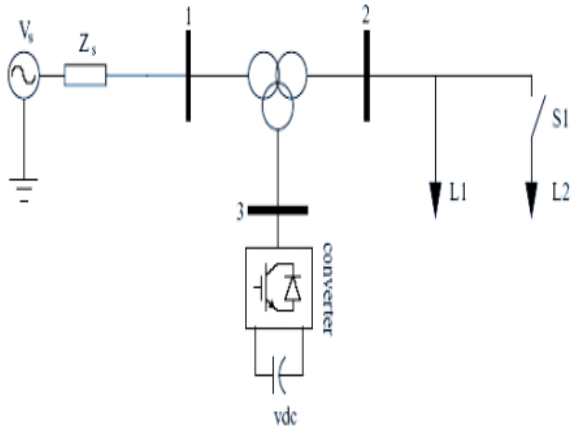

Fig 5 Single line diagram of the test STATCOM

As a result, negative-sequence voltage appears in the supply voltage. This causes a double supply frequency component in the dc-link voltage of the inverter. This double frequency component injects the third harmonic component in the ac side. Moreover, due to negative-sequence voltage, large negative-sequence current flows through the inverter which may cause the STATCOM to trip.

Therefore, during unbalance, the inverter voltages are controlled in such a way that either negative-sequence current flowing into the inverter is eliminated or reduces the unbalance in the grid voltage. In the latter case, STATCOM needs to supply large currents since the interfacing impedance is small. This may lead to trip- ping of the converter.

IV. SIMULATION RESULTS

The system configuration shown in Fig. 1 is considered for simulation. The simulation study is carried out using MATLAB/SIMULINK. The system parameters are given in Table I.

TABLE I SIMULATION SYSTEM PARAMETERS

Rated power	5 MVA
Transformer voltage rating	11kV/400
AC supply frequency, f	50 Hz
Inverter-1 dc link voltage, V_{dc1}	659 V
Inverter-2 dc link voltage, V_{dc2}	241 V
Transformer leakage reactance, X_l	15%
Transformer resistance, R	3%
DC link capacitances, C_1, C_2	50 mF
Switching frequency	1200 Hz

The proposed STATCOM based two level inverter system is studied using MATLAB/ SIMULINK. The overall system configuration and controller are shown

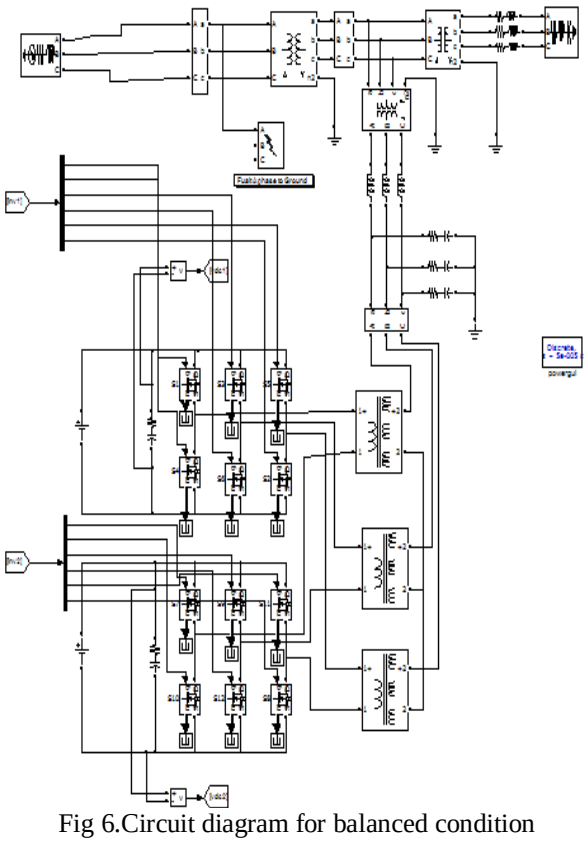

Fig 6.Circuit diagram for balanced condition

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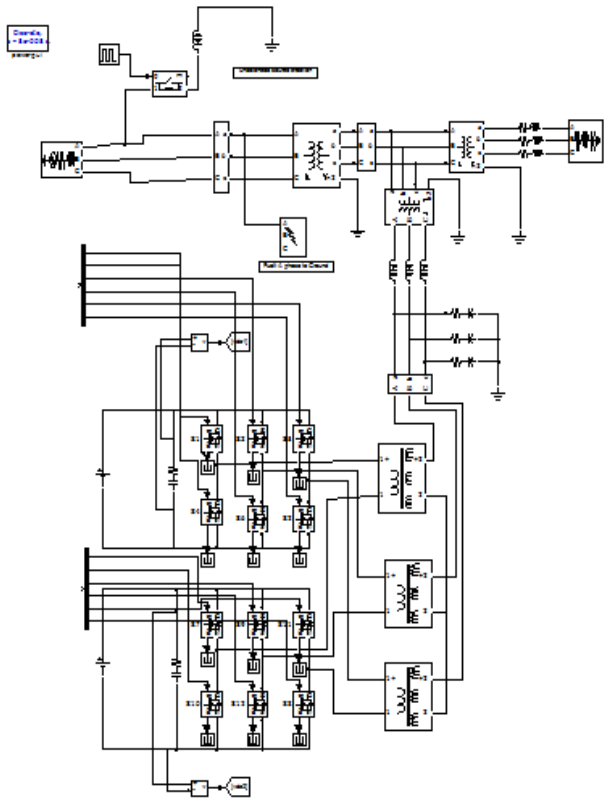


Fig 7. Circuit diagram for unbalanced condition

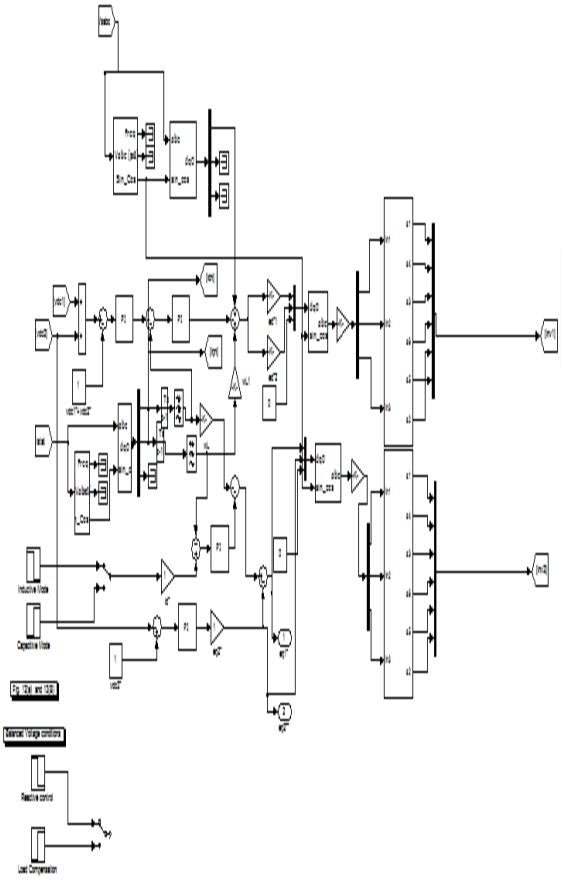
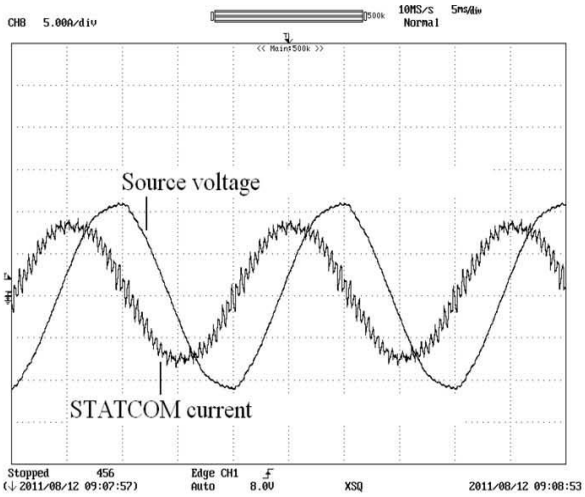
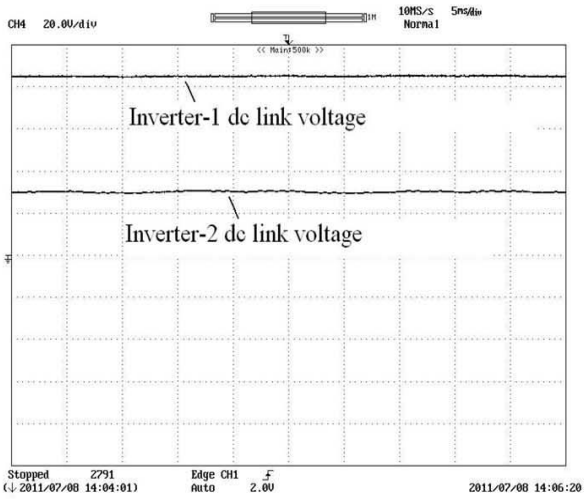


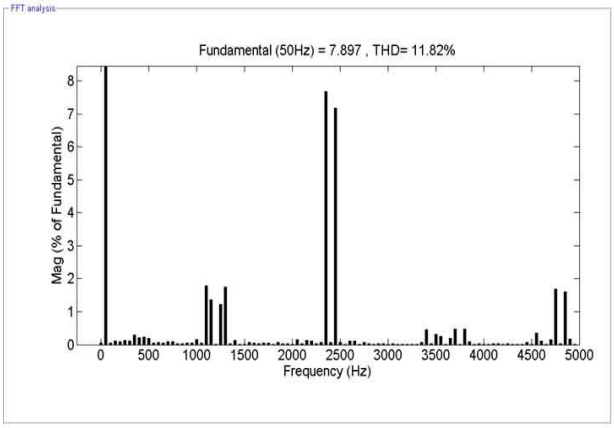
Fig 8. Controller circuit diagram



(a)



(b)



(c)

Fig. 9.1 Experimental result: Capacitive mode of operation. (a) Source voltage (50 V/div) and STATCOM current (5 A/div). (b) DC-link voltages of inverter-1 and inverter-2 (20 V/div). Time scale: 5 ms/div. (c) Harmonic spectrum of current.

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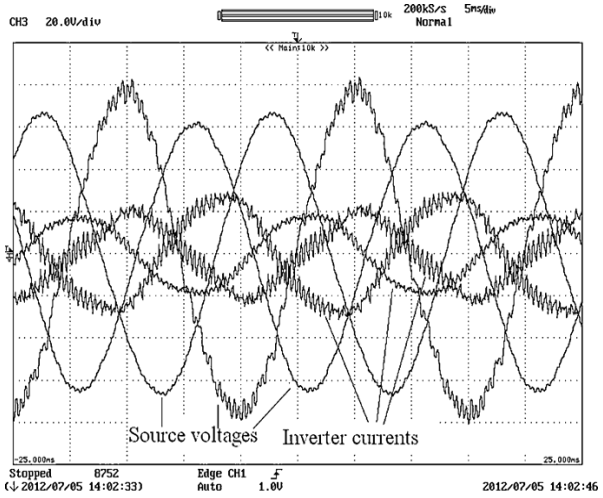
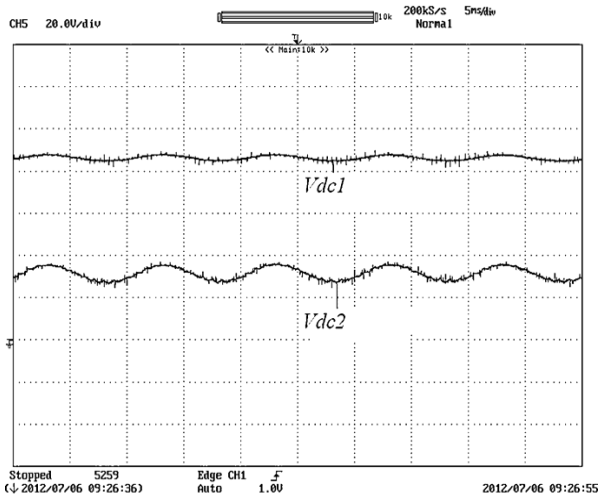


(a)



(b)

Fig. 9.2. Operation under unbalanced voltage conditions and without the negative-sequence controller: (a) Source voltages (20 V/div) and inverter currents (5 A/div). (b) DC-link voltages of inverter-1 and inverter-2 (20 V/div). Time scale: 5 ms/div.

V. CONCLUSION

The DC-link voltage balance is one of the major issues in cascaded inverter-based STATCOMs. In this paper, a simple var compensating scheme is proposed for a cascaded two-level inverter-based multilevel inverter. The scheme ensures regulation of dc-link voltages of inverters at asymmetrical levels and reactive power compensation. The performance of the scheme is validated by simulation and experimentations under balanced and unbalanced voltage conditions. Further, the cause for instability when there is a change in reference current is investigated. The dynamic model is developed and transfer functions are derived. System behavior is analyzed for various operating conditions. From the analysis, it is inferred that the system is a non minimum phase type, that is, poles of the transfer function always lie on the left half of the -plane. However, zeros shift to the right half of the -plane for certain operating conditions. For such a system, oscillatory instability for high controller gains exists.

REFERENCES

[1] Leon, J.M.Mauricio, J. A. Solsona, and A. Gomez-Exposito, "Software sensor-based STATCOM control under unbalanced conditions," IEEE Trans. Power Del., vol. 24, no. 3, pp. 1623–1632, Jul. 2009.

[2] Shukla, A. Ghosh, and A. Joshi, "Hysteresis current control operation of flying capacitor multilevel inverter and its application in shunt compensation of distribution systems," IEEE Trans. Power Del., vol. 22, no. 1, pp. 396–405, Jan. 2007.

[3] Blazic and I. Papic, "Improved D-statcom control for operation with unbalanced currents and voltages," IEEE Trans. Power Del., vol. 21, no. 1,pp. 225–233, Jan. 2006.

[4] Singh, R. Saha, A. Chandra, and K. Al-Haddad, "Static synchronous compensators (STATCOM): A review," IET Power Electron., vol. 2, no. 4, pp. 297–324, 2009.

[5] based control strategy for balancing individual dc capacitor voltages in cascade multilevel inverter-based STATCOM," IEEE Trans. Ind. Electron., vol. 56, no. 6, pp. 2259–2269, Jun. 2009.

[6] Schauder and H. Mehta, "Vector analysis and control of advanced static Var compensators," in Proc. Inst. Elect. Eng. C., Jul. 1993, vol. 140,no. 4, pp. 299–305.

[7] H. Akagi, H. Fujita, S. Yonetani, and Y. Kondo, "A 6.6-kV transformerlessSTATCOMbased on a five-level diode-clamped PWM converter:System design and experimentation of a 200-V 10-kVA laboratory model," IEEE Trans. Ind. Appl., vol. 44, no. 2, pp. 672–680, Mar./Apr.2008.

[8] H. Akagi, S. Inoue, and T. Yoshii, "Control and performance of a transformerless cascaded PWM STATCOM with star configuration," IEEE Trans. Ind. Appl., vol. 43, no. 4, pp. 1041–1049, Jul./Aug. 2007.

[9] H.P.Mohammadi and M.T.Bina,"A transformerless medium-voltage STATCOM topology based on extended modular multilevel converters," IEEE Trans. Power Electron., vol. 26, no. 5, pp. 1534–1545,May 2011.

[10] K. K. Mohaptra, K. Gopakumar, and V. T. Somasekhar, "A harmonic elimination and suppression scheme for an open-end winding induction motor drive," IEEE Trans. Ind. Electron., vol. 50, no. 6, pp. 1187–1198, Dec. 2003.

[11] K. R. Padiyar and A. M. Kulkarni, "Design of reactive current and voltage controller of static condenser," Elect. Power Energy Syst., vol. 19,no. 6, pp. 397–410, 1997.

[12] M. K. Mishra, A. Ghosh, and A. Joshi, "Operation of a DSTATCOM in voltage control mode," IEEE Trans. Power Del., vol. 18, no. 1, pp.258–264, Jan. 2003.

[13] N. N. V. SurendraBabu, D. Apparao, and B. G. Fernandes, "Asymmetrical dc link voltage balance of a cascaded two level inverter based STATCOM," in Proc., IEEE TENCON, 2010, pp. 483–488.

[14] R. Gupta and A.Ghosh, "Frequency-domain characterization of sliding mode control of an inverter used in DSTATCOM application," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 53, no. 3, pp. 662–676, Mar. 2006.

[15] R. Gupta, A. Ghosh, and A. Joshi, "Switching characterization of cascaded multilevel inverter controlled systems," IEEE Trans. Ind. Electron.,vol. 55, no. 3, pp. 1047–1058, Mar. 2008.

[16] X. Kou, K. A. Corzine, and M. W. Wielebski, "Over distention operation of cascaded multilevel inverters," IEEE Trans. Ind. Appl., vol. 42, no.3, pp. 817–824, May/Jun. 2006.

[17] Kawabata, N. Yahata,M. Horii, E. Egiogu, and T. Kawabata, "SVG using open winding transformer and two inverters," in Proc., 35th Annual IEEE Power Electron. Specialists Conf., 2004, pp. 3039–3044.

[18] Y. Suh, Y. Go, and D. Rho, "A comparative study on control algorithm for active front-end rectifier of large motor drives under unbalanced input," IEEE Trans. Ind. Appl., vol. 47, no. 3, pp. 825–835, May/Jun.2011.

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